深圳市一众显示科技有限公司

SHEN ZHEN TEAM SOURCE DISPLAY TECH. CO, LTD.

TFT-LCD Module Specification

Module NO.：TSM043MCWH-01

Version：V1.0

☐ APPROVAL FOR SPECIFICATION   ☐ APPROVAL FOR SAMPLE

For Customer's Acceptance：	
Approved by	**Comment**

Team Source Display：		
Presented by	**Reviewed by**	**Organized by**

Version No.	Date	Content	Remark
V1.0	2018-4-20	Initial Release	

Contents

Item	Dimension	Unit
Dot Matrix	480 x RGBx272(TFT)	dots
Module dimension	105.5x 67.2 x 6.2	mm
View area	95.04x 53.85	mm
Dot pitch	0.066(W) × 0.198(H)	mm
LCD type	TFT, Negative, Transmissive	
View Direction	12 o'clock	
Gray Scale Inversion Direction	6 o'clock	
Backlight Type	LED,Normally White (1x7 LEDs)	
Driver IC	SSD1963	

*Expose the IC number blaze (Luminosity over than 1 cd) when using the LCM may cause IC operating
 failure.

*Color tone slight changed by temperature and driving voltage.

2.Block Diagram
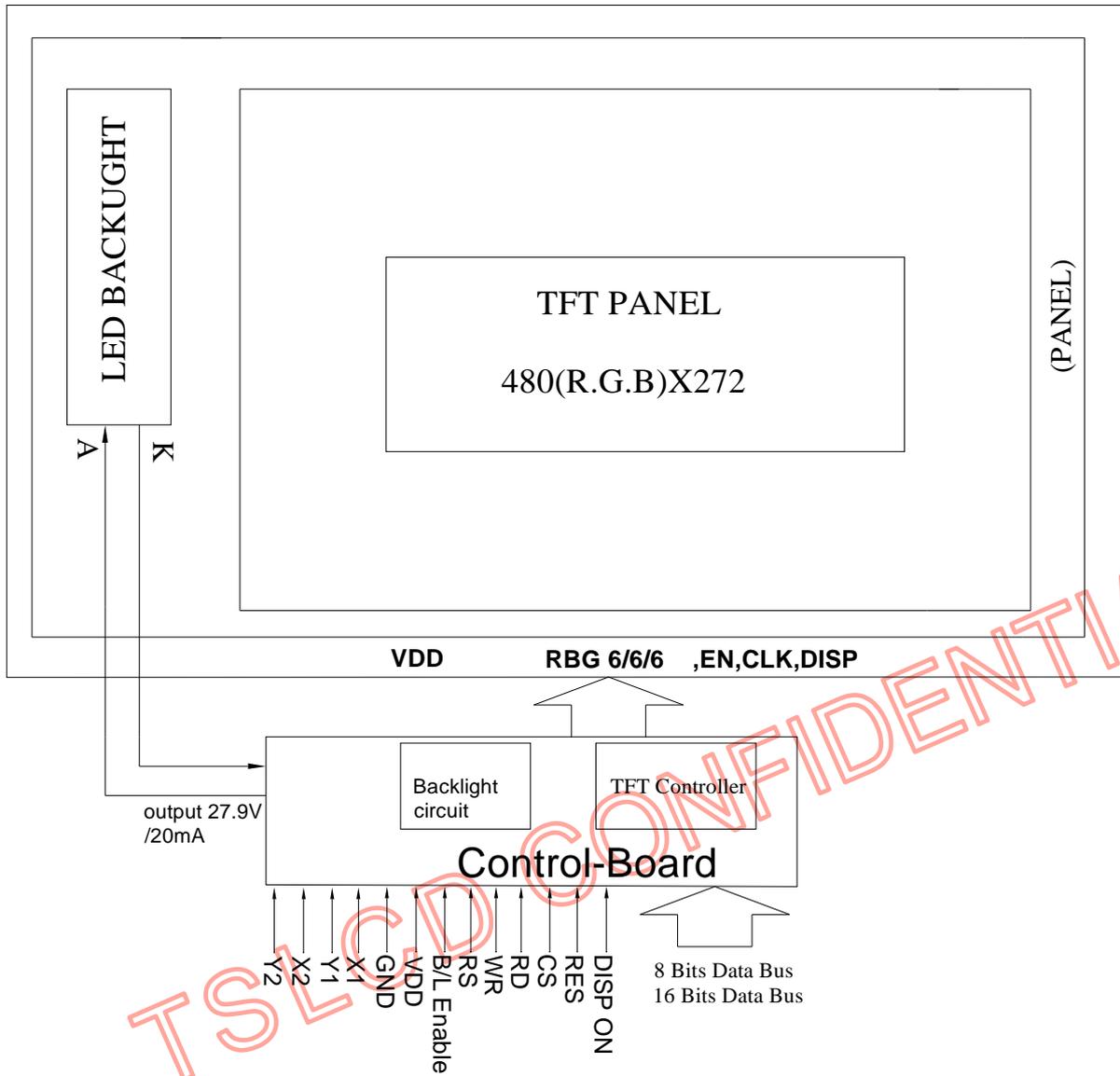
3.Electrical Characteristics

Item	Symbol	Values			Unit	Remark
		Min	TYP	max		
Operating voltage	VDD	3.1	3.3	3.5	V	
Input high voltage	VIH	0.8*VDD	-	VDD	V	
Input low voltage	VIL	0	-	0.2*VDD	V	
Output high voltage	VOH	VDD-0.3		VDD	V	
Output low voltage	VOL	0	-	0.3	V	
Current Consumption	IVCI	-	245	-	mA	
Power Consumption	PLCD	-	808.5	-	mW	

4.Absolute Maximum Ratings

| Item	Symbol	Values		Unit	Remark
		Min	max		
Power Supply Voltages	VDD	-0.5	5.0	V	
Input signal voltage	Logic input	-0.5	5.0	V	
Operating Temperature	Topa	-20	70	°C	Note3,4
Storage Temperature	Tst	-30	80	°C	Note3,4
LED Reverse Voltage	Vr	-	1.2	V	Each LED Note2
LED Forward Current	IF	-	25	mA	Each LED
LED life time	--	20,000	--	--	Note5

Note 1: The absolute maximum rating values of this product are not allowed to be exceeded at any times.
A module should be used with any of the absolute maximum ratings exceeded, the characteristics of the
module may not be recovered, or in an extreme condition, the module may be permanently destroyed.
Note 2: VR Conditions: Zener Diode 20mA
Note 3: 90% RH Max. (Max wet temp. is 60℃)
Maximum wet-bulb temperature is at 60℃ or less. And No condensation (no drops of dew)
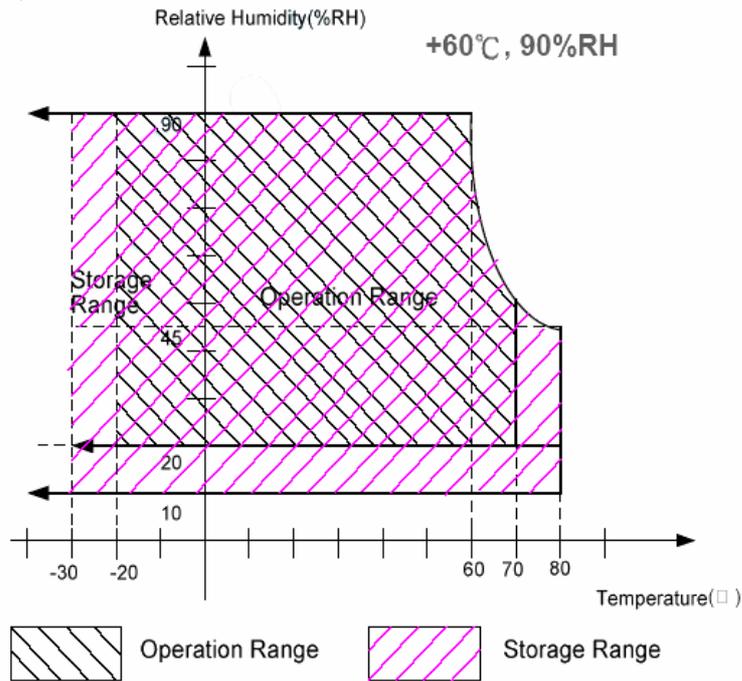
Note 4: In case of temperature below 0℃,the response time of liquid crystal (LC) becomes slower and the color of panel darker than normal one.

Note 5: The "LED life time" is defined as the module brightness decrease to 50% original brightness that the ambient temperature is 25℃ and IL =20mA. The LED lifetime could be decreased if operating IL is lager than 20 mA.

5.Interface Pin Function

5.1   Pins Connection To Control Board

P/N	Symbol	16BIT Function	P/N	Symbol	16BIT Function
1	GND	Ground	26	RST	Reset
2	VCC	Power supply for Logic	27	NC	No connection
3	BL_E	Backlight Enable	28	NC	No connection
4	RS		29	NC	No connection
5	WR	8080 family MPU interface : Write signal	30	NC	No connection
6	RD	8080 family MPU interface: Read signal	31	NC	No connection
7	DB0	Data bus	32	DISP	DISPLAY ON(1) / OFF(0)
8	DB1				
9	DB2				
10	DB3				
11	DB4				
12	DB5				
13	DB6				
14	DB7				
15	DB8				
16	DB9				
17	DB10				
18	DB11				
19	DB12				
20	DB13				
21	DB14				
22	DB15				
23	NC	No connection			
24	NC	No connection			
25	CS	Chip select			

6. DC CHARATERISTICS

Conditions:

Voltage referenced to VSS

VDDD, VDDPLL = 1.2V

VDDIO, VDDLCD = 3.3V

TA = 25°C

DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
PSTY	Quiescent Power			300	500	uW
IIZ	Input leakage current		-1		1	uA
IOZ	Output leakage current		-1		1	uA
VOH	Output high voltage		0.8VDDIO			V
VOL	Output low voltage				0.2VDDIO	V
VIH	Input high voltage		0.8VDDIO		VDDIO + 0.5	V
VIL	Input low voltage				0.2VDDIO	V

7. AC Characteristics

Conditions:

Voltage referenced to VSS

VDDD, VDDPLL = 1.2V

VDDIO, VDDLCD = 3.3V

TA = 25°C

CL = 50pF (Bus/CPU Interface)

CL = 0pF (LCD Panel Interface)

7.1 Clock Timing

Table 7-1:Clock Input Requirements for CLK (PLL-bypass)

Symbol	Parameter	Min	Max	Units
FCLK	Input Clock Frequency (CLK)		110	MHz
TCLK	Input Clock period (CLK)	1/fCLK		ns

Table 7-2:Clock Input Requirements for CLK

Symbol	Parameter	Min	Max	Units
FCLK	Input Clock Frequency (CLK)	2.5	50	MHz
TCLK	Input Clock period (CLK)	1/fCLK		ns

Table 7-3:Clock Input Requirements for crystal oscillator XTAL

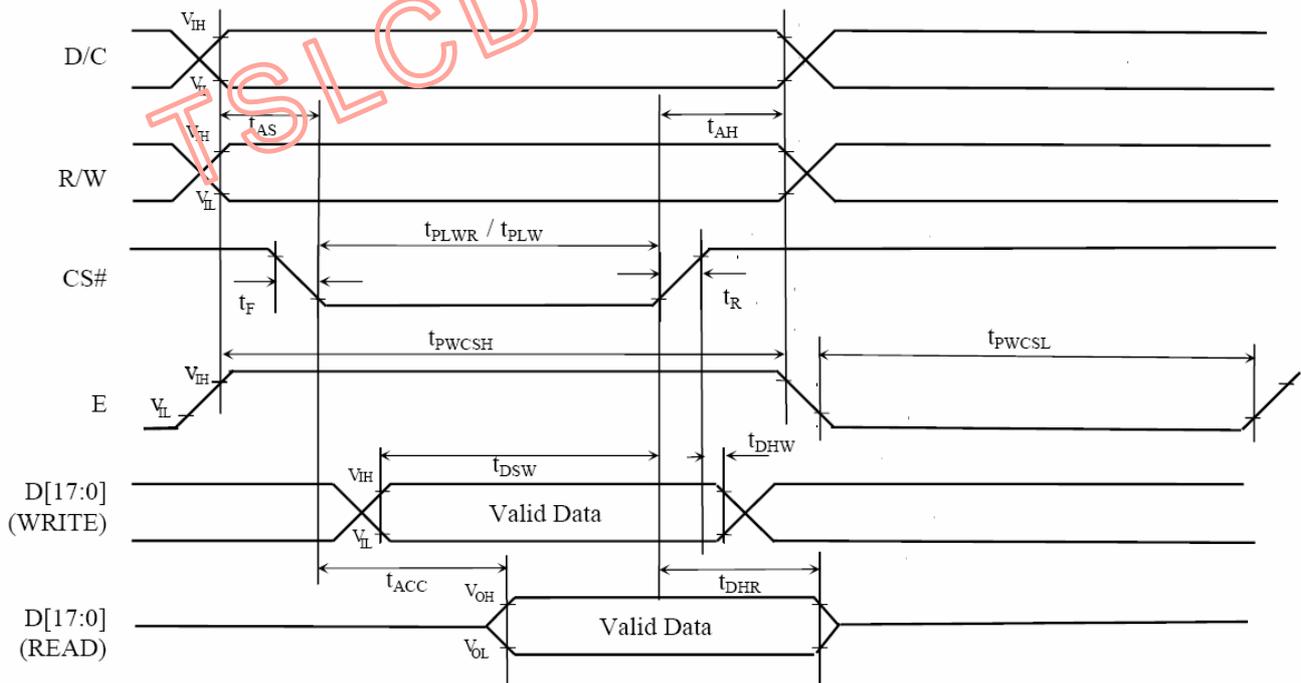| Symbol	Parameter	Min	Max	Units
FXTAL	Input Clock Frequency	2.5	10	MHz
TXTAL	Input Clock period	1/fXTAL		ns

7.2 MCU Interface Timing

7.2.1 Parallel 6800-series Interface Timing

Table 7-4: Parallel 6800-series Interface Timing Characteristics (Use CS# as clock)

Symbol	Parameter		Min	Typ	Max	Unit
fMCLK	System Clock Frequency*		1	-	110	MHz
tMCLK	System Clock Period*		1/ fMCLK	-	-	ns
tPWCSH	Control Pulse High Width	Write	13	1.5* tMCLK	-	ns
		Read	30	3.5* tMCLK		
tPWCSL	Control Pulse Low Width	Write (next write cycle)	13	1.5* tMCLK	-	ns
		Write (next read cycle)	80	9* tMCLK		
		Read	80	9* tMCLK		
tAS	Address Setup Time		2	-	-	ns
tAH	Address Hold Time		2	-	-	ns
tDSW	Data Setup Time		4	-	-	ns
tDHW	Data Hold Time		1	-	-	ns
tPLW	Write Low Time		14	-	-	ns
tPHW	Write High Time		14	-	-	ns
tPLWR	Read Low Time		38	-	-	ns
tACC	Data Access Time		32	-	-	ns
tDHR	Output Hold time		1	-	-	ns
tR	Rise Time		-	-	0.5	ns
tF	Fall Time		-	-	0.5	ns

* System Clock denotes external input clock (PLL-bypass) or internal generated clock (PLL-enabled)

Figure 7-1: Parallel 6800-series Interface Timing Diagram (Use CS# as Clock)
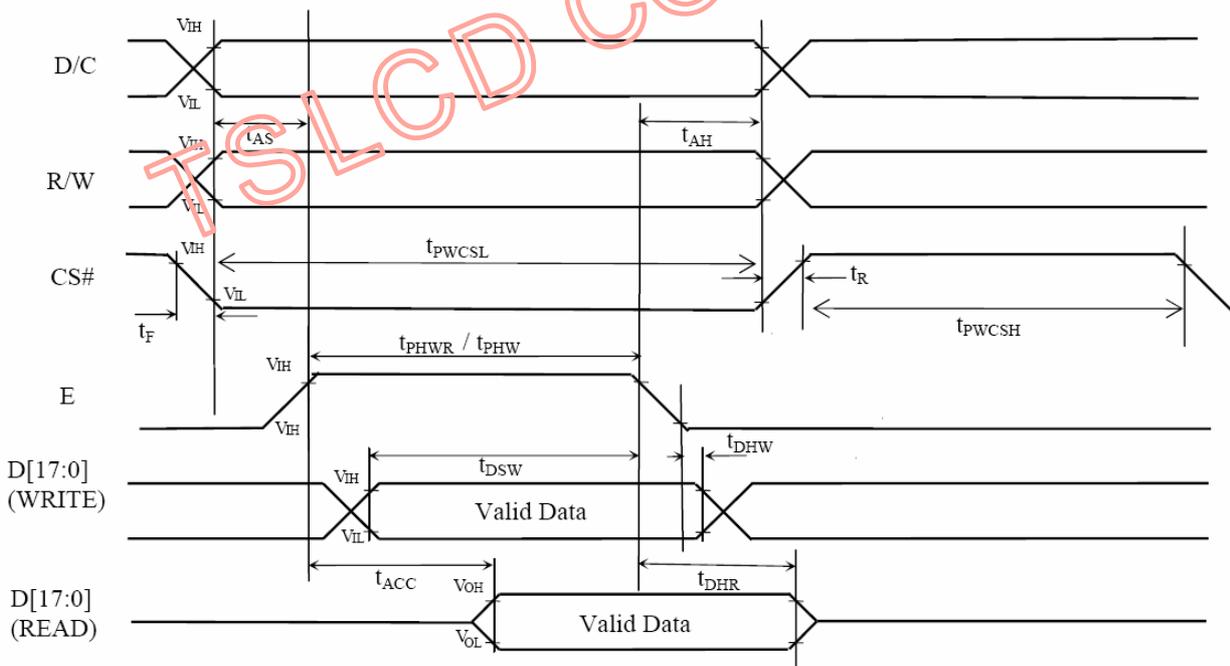
Table 7-5: Parallel 6800-series Interface Timing Characteristics (Use E as clock)

Symbol	Parameter		Min	Typ	Max	Unit
fMCLK	System Clock Frequency*		1	-	110	MHz
tMCLK	System Clock Period*		1/ fMCLK	-	-	ns
tPWCSH	Control Pulse Low Width	Write (next write cycle)	13	1.5* tMCLK	-	ns
		Write (next read cycle)	80	9* tMCLK		
		Read	80	9* tMCLK		
tPWCSL	Control Pulse High Width	Write	13	1.5* tMCLK	-	ns
		Read	30	3.5* tMCLK		
tAS	Address Setup Time		2	-	-	ns
tAH	Address Hold Time		2	-	-	ns
tDSW	Data Setup Time		4	-	-	ns
tDHW	Data Hold Time		1	-	-	ns
tPLW	Write Low Time		14	-	-	ns
tPHW	Write High Time		14	-	-	ns
tPLWR	Read Low Time		38	-	-	ns
tACC	Data Access Time		32	-	-	ns
tDHR	Output Hold time		1	-	-	ns
tR	Rise Time		-	-	0.5	ns
tF	Fall Time		-	-	0.5	ns

* System Clock denotes external input clock (PLL-bypass) or internal generated clock (PLL-enabled)

Figure7-2: Parallel 6800-series Interface Timing Diagram (Use E as Clock)

7.2.2 Parallel 8080-series Interface Timing

Table 7-6: Parallel 8080-series Interface

Symbol	Parameter		Min	Typ	Max	Unit
fMCLK	System Clock Frequency*		1	-	110	MHz
tMCLK	System Clock Period*		1/ fMCLK	-	-	ns
tPWCSL	Control Pulse High Width	Write	13	1.5* tMCLK	-	ns
		Read	30	3.5* tMCLK		
tPWCSH	Control Pulse Low Width	Write (next write cycle)	13	1.5* tMCLK	-	ns
		Write (next read cycle)	80	9* tMCLK		
		Read	80	9* tMCLK		
tAS	Address Setup Time		1	-	-	ns
tAH	Address Hold Time		2	-	-	ns
tDSW	Write Data Setup Time		4	-	-	ns
tDHW	Write Data Hold Time		1	-	-	ns
tPWLW	Write Low Time		12	-	-	ns
tDHR	Read Data Hold Time		1	-	-	ns
tACC	Access Time		32	-	-	ns
tPWLR	Read Low Time		36	-	-	ns
tR	Rise Time		-	-	0.5	ns
tF	Fall Time		-	-	0.5	ns
tCS	Chip select setup time		2	-	-	ns
tCSH	Chip select hold time to read signal		3	-	-	ns

* System Clock denotes external input clock (PLL-bypass) or internal generated clock (PLL-enabled)

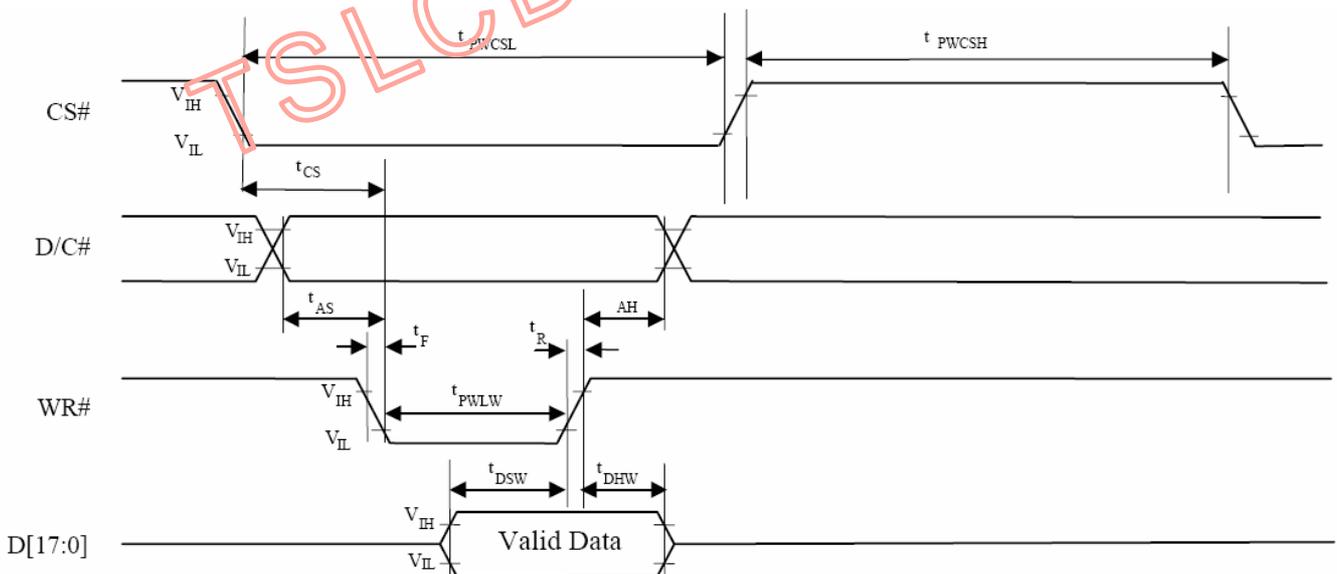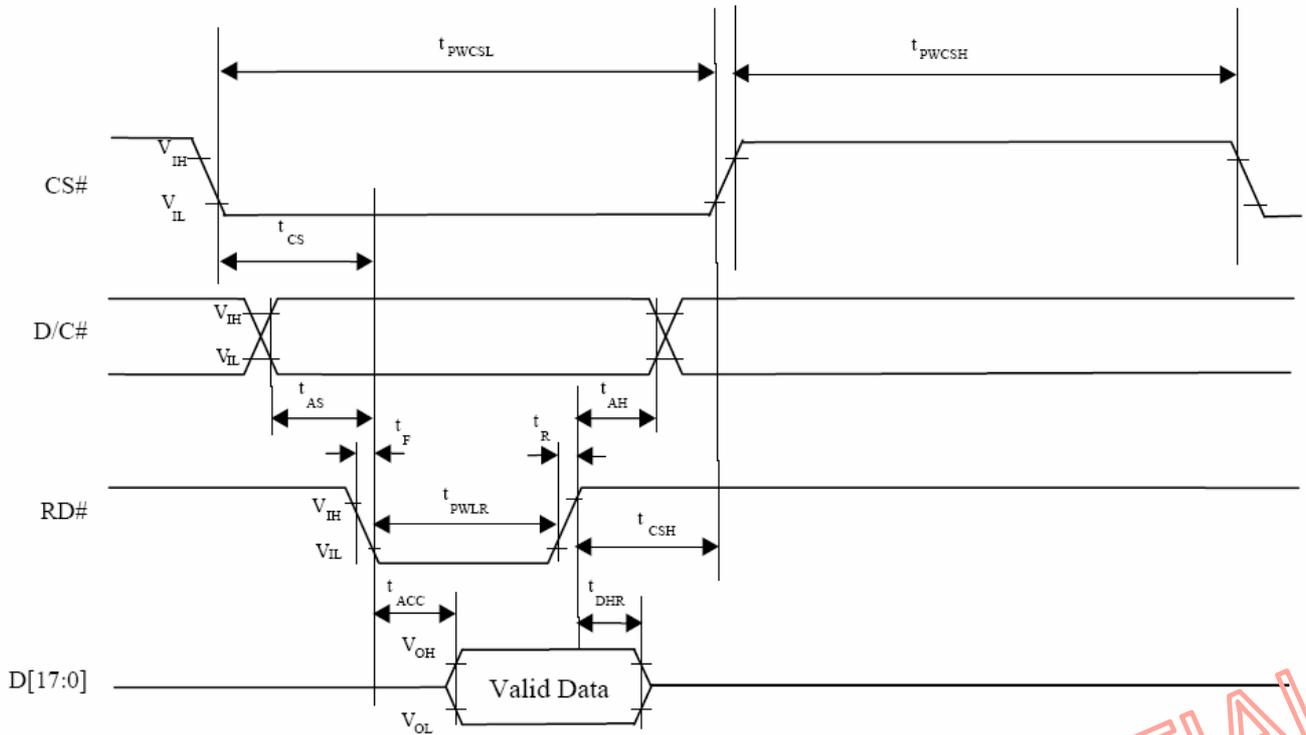### Figure 7-3: Parallel 8080-series Interface Timing Diagram (Write Cycle)

Figure 7-4: Parallel 8080-series Interface Timing Diagram (Read Cycle)

8. Data transfer order setting

Pixel Data Format

Both 6800 and 8080 support 8-bit, 9 bit,16 bit, 18 bit and 24 bit data bus. Depending on the width of the data bus, the display data are packed into the data bus in the different ways.

Table 8-1: Pixel Data Format

Interface	Cycle	D[0]	D[1]	D[2]	D[3]	D[4]	D[5]	D[6]	D[7]	D[8]	D[9]	D[10]	D[11]	D[12]	D[13]	D[14]	D[15]	D[16]	D[17]	D[18]	D[19]	D[20]	D[21]	D[22]	D[23]
24 bits	1st	B0	B1	B2	B3	B4	B5	B6	B7	G0	G1	G2	G3	G4	G5	G6	G7	R0	R1	R2	R3	R4	R5	R6	R7
18 bits	1st	B0	B1	B2	B3	B4	B5	G0	G1	G2	G3	G4	G5	R0	R1	R2	R3	R4	R5						
16 bits (565 format)	1st	B1	B2	B3	B4	B5	G0	G1	G2	G3	G4	G5	R1	R2	R3	R4	R5								
16 bits	1st	G0	G1	G2	G3	G4	G5	G6	G7	R0	R1	R2	R3	R4	R5	R6	R7								
16 bits	2nd	R0	R1	R2	R3	R4	R5	R6	R7	B0	B1	B2	B3	B4	B5	B6	B7								
16 bits	3rd	B0	B1	B2	B3	B4	B5	B6	B7	G0	G1	G2	G3	G4	G5	G6	G7								
12 bits	1st	G4	G5	G6	G7	R0	R1	R2	R3	R4	R5	R6	R7												
12 bits	2nd	B0	B1	B2	B3	B4	B5	B6	B7	G0	G1	G2	G3												
9 bits	1st	G3	G4	G5	R0	R1	R2	R3	R4	R5															
9 bits	2nd	B0	B1	B2	B3	B4	B5	G0	G1	G2															
8 bits	1st	R0	R1	R2	R3	R4	R5	R6	R7																
8 bits	2nd	G0	G1	G2	G3	G4	G5	G6	G7																
8 bits	3rd	B0	B1	B2	B3	B4	B5	B6	B7																

9 Register Depiction

Please consult the spec of SSD1963 Version 1.2

10. OPTICAL CHARATERISTIC

Item	Symbol	Condition	Values			Unit	Remark
			Min.	Typ.	Max.		
Viewing angle (CR$\geq$10)	θ_L	$\varphi=180^0$(9 o'clock)	60	70	—	degree	Note1
	θ_R	$\varphi=0^0$(3 o'clock)	60	70	—		
	θ_T	$\varphi=90^0$(12 o'clock)	40	50	—		
	θ_B	$\varphi=270^0$(6 o'clock)	60	70	—		
Response time	T_{ON}		—	10	20	msec	Note 3
	T_{OFF}		—	15	30	msec	Note 3
Contrast ratio	CR		400	500	—	—	Note 4
Color chromaticity	W_X	Normal $\theta=\varphi=0^0$	0.26	0.31	0.36	—	Note 2 Note 5 Note 6
	W_Y		0.28	0.33	0.38	—	
Luminance	L		280	300	—	Cd/m^2	Note 6
Luminance uniformity	Yu		70	75	—	%	Note 7

Note 1: Definition of viewing angle range
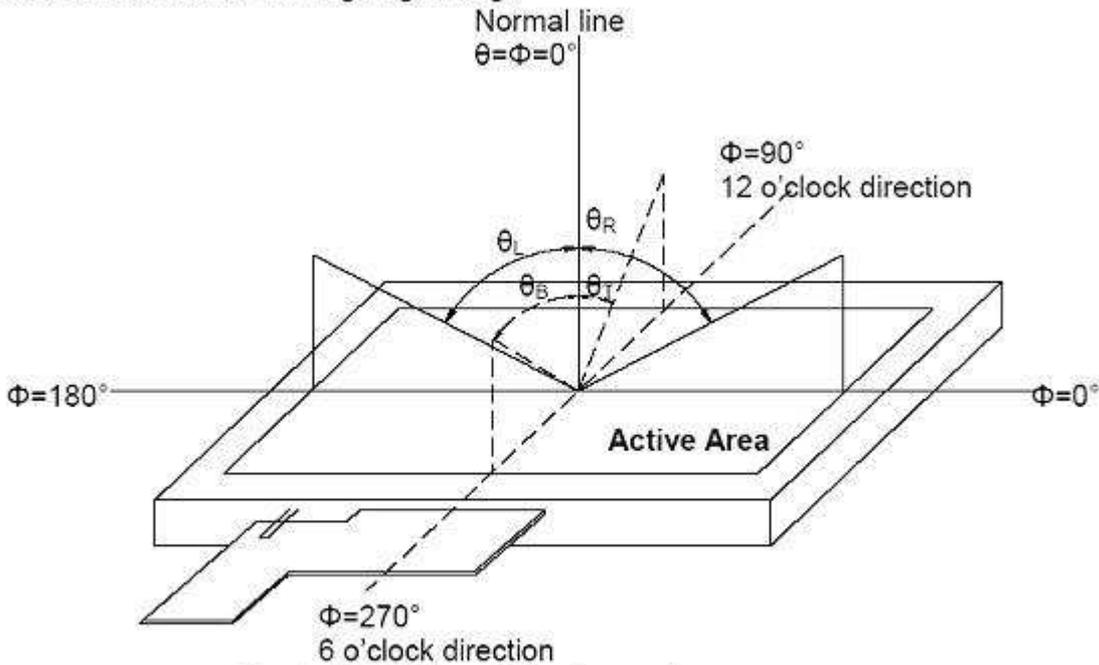
Fig. 4-1 Definition of viewing angle

Note 2: Definition of optical measurement system.
The optical characteristics should be measured in dark room. After 30 minutes operation, the optical properties are measured at the center point of the LCD screen. (Response time is measured by Photo detector TOPCON BM-7, other items are measured by BM-5A/Field of view: 1° /Height: 500mm)
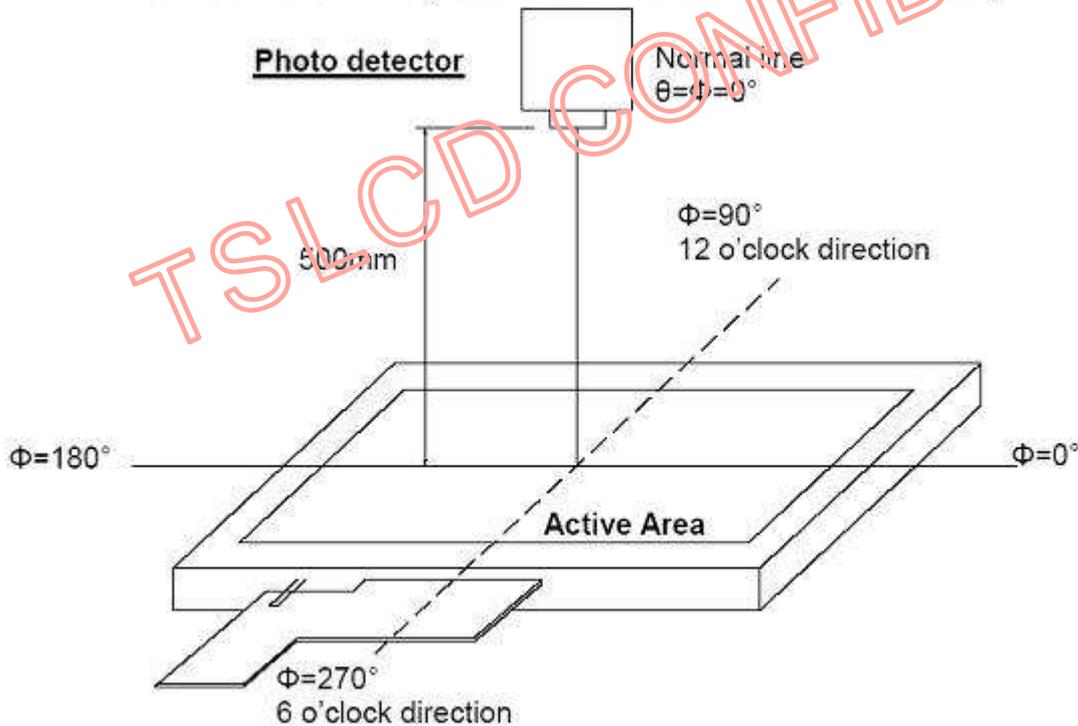
Fig. 4-2 Optical measurement system setup

Note 3: Definition of Response time
    The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T$_{ON}$) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T$_{OFF}$) is the time between photo detector output intensity changed from 10% to 90%.
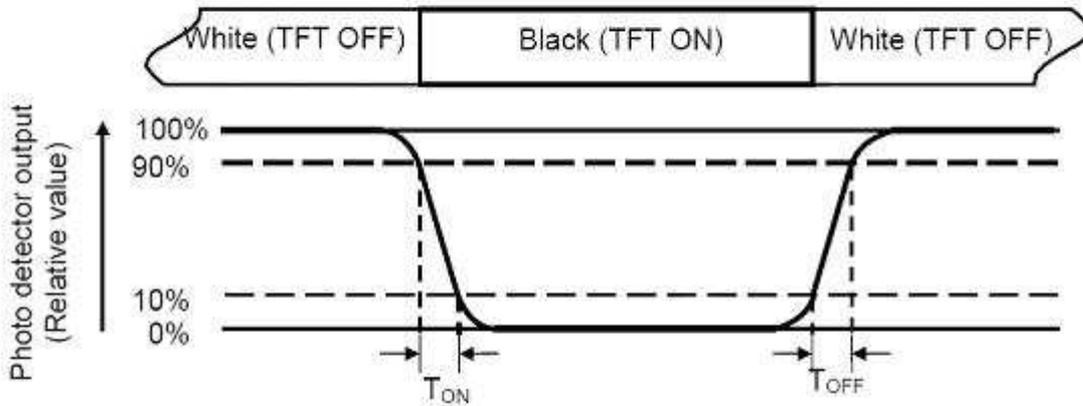
Fig. 4-3 Definition of response time

Note 4: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of color chromaticity (CIE1931)
    Color coordinates measured at center point of LCD.
Note 6: All input terminals LCD panel must be ground while measuring the center area of the panel. The LED driving condition is I$_L$=20mA.

Note 7: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer to Fig. 4-4).Every measuring point is placed at the center of each measuring area.

$$Luminance\ Uniformity\ (Yu) = \frac{B_{min}}{B_{max}}$$

L-------Active area length   W----- Active area width
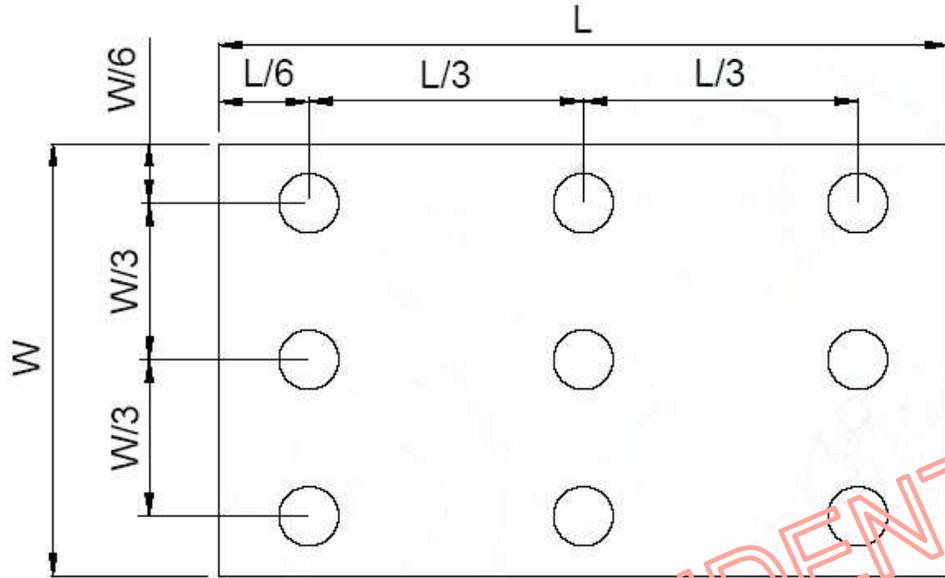
Fig. 4-4 Definition of measuring points

B_{max}: The measured maximum luminance of all measurement position.
B_{min}: The measured minimum luminance of all measurement position.

11　Outline drawings

GENERAL TOLERANCE±0.2

LCD Type	4.3"TFT,Transmissive, Normally white,TN
Resolution	480(RGB)*272
View Direction	12 OCLOCK
Driver IC	SSD1963
Color Depth	16.7M
Interface Types	MCU8-bit
Operating voltage	VCC=3.3V
With/without TP	Without
Backlight LEDs	7 LEDs, 20mA
Surface luminance	300cd/m²
Operating temperature	-20℃~70℃
Storage Temperature	-30℃~80℃

LED CIRCUIT DIAGRAM 22.4V@20mA

Pixtel Detail

LCM INPUT PIN

Pin NO.	Symbol
1	GND
2	VCC
3	BL_EN
4	RS
5	WR
6	RD
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	DB8
16	DB9
17	DB10
18	DB11
19	DB12
20	DB13
21	DB14
22	DB15
23	NC
24	NC
25	CS
26	RESET
27	NC
28	NC
29	NC
30	NC
31	NC
32	DISP/NC

产品型号 (Product Model): TSM043MCWH-01　版本 (Version): V1

设计 (DESIGN): Aron 2017.10.31　审核 (AUDITING): Penix 2017.10.31　批准 (APPROVED):

东莞市一众显示科技有限公司　DONG GUAN TEAM SOURCE DISPLAY TECH. CO., LTD.

12.Reliability Test

WIDE TEMPERATURE RELIABILITY TEST

N O.	ITEM	CONDITION			STANDARD	NOTE
1	High Temp. Storage	80℃	240 Hrs		Appearance without defect	
2	Low Temp. Storage	-30℃	240 Hrs		Appearance without defect	
3	High Temp. & High Humi. Storage	60 ℃ 90%RH	240 Hrs		Appearance without defect	
4	High Temp. Operating Display	70℃	240 Hrs		Appearance without defect	
5	Low Temp. Operating Display	-20℃	240 Hrs		Appearance without defect	
6	Thermal Shock	-20 ℃, 30min. → 70℃, 30min. (1cycle)			Appearance without defect	10 cycles

Inspection Provision

1.Purpose

The TSLCD's inspection provision provides outgoing inspection provision and its expected quality level based on our outgoing inspection of TS Display LCD Produces.

2.Applicable Scope

The WINSTAR inspection provision is applicable to the arrangement in regard to outgoing inspection and quality assurance after outgoing.

3.Technical Terms

3-1 WINSTAR Technical Terms

4.Outgoing Inspection

4-1 Inspection Method

MIL-STD-105E Level Ⅱ Regular inspection

4-2 Inspection Standard

		Item	AQL(%)	Remarks
Major Defect	Dots	Opens Shorts Erroneous operation	0.4	Faults which substantially lower the practicality and the initial purpose difficult to achieve
	Solder appearance	Shorts Loose		
	Cracks	Display surface cracks		

			AQL	
	Dimensions	External from Dimensions	0.4	
Minor Defect	Inside the glass	Black spots	0.65	Faults which appear to pose almost no obstacle to the practicality, effective use, and operation
	Polarizing plate	Scratches, foreign Matter, air bubbles, and peeling		
	Dots	Pinhole, deformation		
	Color tone	Color unevenness		
	Solder appearance	Cold solder Solder projections		

4-3 Inspection Provisions
*Viewing Area Definition

Fig. 1
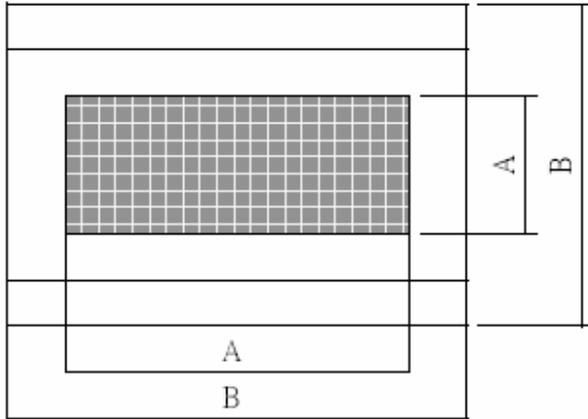
A : Zone Viewing Area
B : Zone Glass Plate Outline

*Inspection place to be 500 to 1000 lux illuminance uniformly without glaring.
The distance between luminous source(daylight fluorescent lamp and cool white fluorescent lamp)
and sample to be 30 cm to 50 cm.

*Test and measurement are performed under the following conditions, unless otherwise specified.
Temperature $20 \pm 15℃$
Humidity $65 \pm 20\%$R.H.
Pressure   860~1060hPa(mmbar)
In case of doubtful judgment, it is performed under the following conditions.
Temperature $20 \pm 2℃$
Humidity $65 \pm 5\%$R.H.
Pressure   860~1060hPa(mmbar)

5.Specification for quality check

5-1-1 Electrical characteristics :

NO.	Item	Criterion
1	Non operational	Fail
2	Miss operating	Fail
3	Contrast irregular	Fail
4	Response time	Within Specified value

5-1-2 Components soldering :

Should be no defective soldering such as shorting, loose terminal cold solder, peeling of printed circuit board pattern, improper mounting position, etc.

5-2 Inspection Standard for TFT panel

5-2-1 The environmental condition of inspection :

The environmental condition and visual inspection shall be conducted as below.

(1) Ambient temperature : 25±5℃

(2) Humidity : 25~75% RH

(3) External appearance inspection shall be conducted by using a single 20W fluorescent lamp or equivalent illumination.

(4) Visual inspection on the operation condition for cosmetic shall be conducted at the distance 30cm or more between the LCD panels and eyes of inspector. The viewing angle shall be 90 degreeto the front surface of display panel.

(5) Ambient Illumination : 300~500 Lux for external appearance inspection.

(6) Ambient Illumination : 100~200 Lux for light on inspection.

5-2-2 Inspection Criteria

(1) Definition of dot defect induced from the panel inside

a) The definition of dot : The size of a defective dot over 1/2 of whole dot is regarded as one defective dot

b) Bright dot : Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

c) Dark dot : Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue pattern.

d) 2 dot adjacent = 1 pair = 2 dots

Picture :

2 dot adjacent   2 dot adjacent (vertical)   2 dot adjacent (slant)
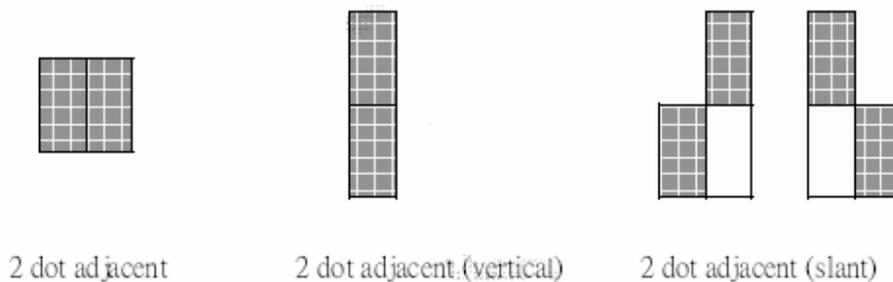
(2) Display Inspection

NO.	Item			Acceptable Count
1	Dot defect	Bright Dot	Random	N $\leqq$ 2
			2 dots adjacent	N $\leqq$ 0
		Dark Dot	Random	N $\leqq$ 3
			2 dots adjacent	N $\leqq$ 1
		Total bright and dark dot		N $\leqq$ 4
	Functional failure (V-line/ H-line/Cross line etc.)			Not allowable
	Mura	It's OK if mura is slight visible through 6% ND filter. (Judged by limit sample if it is necessary)		
2	Newton ring (touch panel)	Orbicular of interference fringes is not allowed in the optimum contrast within the active area under viewing angle.		

(3) Appearance inspection

NO.	Item	Standards
1	Panel Crack	Not allow. It is shown in Fig.1.
2	Broken CF Non -lead Side of TFT	The broken in the area of W > 2mm is ignored, L is ignored. It is shown in Fig.2.
3	Broken Lead Side of TFT	FPC lead, electrical line or alignment mark can't be damaged. It is shown in Fig.3.
4	Broken Corner of TFT at Lead Side	FPC lead. electrical line or alignment mark can't be damaged. It is shown in Fig.4.
5	Burr of TFT / CF Edge	The distance of burr from the edge of TFT / CF, W $\leqq$ 0.3mm. It is shown in Fig.5.
6	Foreign Black / White/Bright Spot	(1) 0.15 < D $\leqq$ 0.5 mm, N$\leqq$ 4 ; (2) D $\leqq$ 0.15mm, Ignore. It is shown in Fig.6.
7	Foreign Black / White/Bright Line	(1) 0.05<W$\leqq$ 0.1 mm, 0.3<L$\leqq$2 mm, N$\leqq$ 4.
		(2) W $\leqq$ 0.05mm and L$\leqq$ 0.3mm Ignore.
		It is shown in Fig.7.
8	Color irregular	Not remarkable color irregular.

NOTICE:
・ SAFETY
1. If the LCD panel breaks, be careful not to get the liquid crystal to touch your skin.
2. If the liquid crystal touches your skin or clothes, please wash it off immediately by using soap and water.

・ HANDLING
1. Avoid static electricity which can damage the CMOS LSI.
2. Do not remove the panel or frame from the module.
3. The polarizing plate of the display is very fragile. So, please handle it very carefully.
4. Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.
5. Do not use ketonics solvent & Aromatic solvent. Use a soft cloth soaked with a cleaning naphtha solvent.

・ STORAGE
1. Store the panel or module in a dark place where the temperature is 25±5℃ and the humidity is below 65% RH.
2. Do not place the module near organics solvents or corrosive gases.
3. Do not crush, shake, or jolt the module.

・ TERMS OF WARRANT
1. Acceptance inspection period
The period is within one month after the arrival of contracted commodity at the buyer's factory site.
2. Applicable warrant period
The period is within twelve months since the date of shipping out under normal using and storage conditions.

Packing

PARAMETER	Specification	Unit
Outside box	390(L) x 350(W) x 480(H)	mm
Inside pearl wool box	375(L) x 340(W) x 100(H)	mm
Product quantity of Inside box	36	pcs
Total product quantity	36*4=144	pcs
Total weight	15 ±0.5	Kg