深圳市一众显示科技有限公司

SHEN ZHEN TEAM SOURCE DISPLAY TECH. CO, TD.

TFT-LCD Module Specification

Module NO.：TST050HDHI-20

Version：V1.0

☐ APPROVAL FOR SPECIFICATION　　☐ APPROVAL FOR SAMPLE

For Customer's Acceptance：	
Approved by	**Comment**

Team Source Display：		
Presented by	**Reviewed by**	**Organized by**

Version No.	Date	Content	Remark
V1.0	2018-1-15	Initial Release	

CONTENTS

website: www.tslcd.com   www.lcdlcm.com   Email: tslcd@tslcd.com

1   General Characteristics

ITEM	Specification	Unit
LCD Type	a-Si TFT,Transmissive,Normally black,IPS	-
LCD Size	5.0	inch
Resolution (W x H)	720x (RGB) × 1280	pixel
LCM (W × H × D)	65.3(W) x 119.3(H) x 1.65(D)	mm
Active Area (W × H)	62.1 (W) x 110.4 (H)	mm
Dot Pitch (W × H)	0.08625 (H)* 0.08625 (V)	mm
Viewing Direction	All o'clock	-
Gray Scale Inversion Direction	-	-
Viewing Angle	Top/Bottom/ Left/ Right:80	deg.
Color Depth	16.7M	-
Pixel Arrangement	RGB-stripe	-
Backlight Type	12 LEDs，40mA,18.6V	-
Surface Luminance	300	cd/m2
Surface Treatment	Glossy	-
Driver IC	ILI9881C-0D	-
Interface Type	MIPI-4Lane, Video mode	-
Input Voltage	2.8	V
With/Without TP	without	-
Weight	TBD	g

Note 1: RoHS compliant

Note 2: LCM weight tolerance: ± 5%.

2   Product drawings

3 Interface description

PIN NO.	Symbol	Description
1	LED-A	Backlight anode input pin.
2	LEDK	Backlight Cathode input pin.
3	LEDK	Backlight Cathode input pin.
4	VDD	Power supply: +2.8V
5	RESET	Reset input signal
6	+5V (VSP)	Input voltage from step-up circuit. Connect to an external power supply of 4.5V to 6.6V
7	-5V (VSN)	Input voltage from step-up circuit. Connect to an external power supply of -4.5V to -6.6V.
8	IOVCC	Power supply for I/O: +2.8V/1.8V; IOVCC≤VDD
9	GND	System Ground. (0V)
10	GND	System Ground. (0V)
11	D0N	MIPI DSI differential data pair. (Data lane 0)
12	D0P	
13	GND	System Ground. (0V)
14	D1N	MIPI DSI differential data pair. (Data lane 1)
15	D1P	
16	GND	System Ground. (0V)
17	TCN	MIPI DSI differential clock pair
18	TCP	
19	GND	System Ground. (0V)
20	D2N	MIPI DSI differential data pair. (Data lane 2)
21	D2P	
22	GND	System Ground. (0V)
23	D3N	MIPI DSI differential data pair. (Data lane 3)
24	D3P	
25	GND	System Ground. (0V)

4 LCM Interface Timing

4.1 Reset Timing
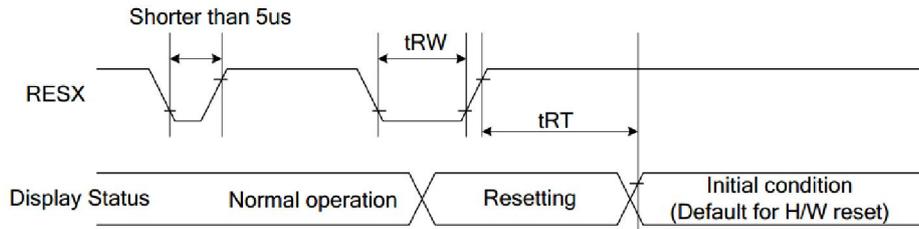
Signal	Symbol	Parameter	Min	Max		Unit
RESX	tRW	Reset pulse duration	10	-		us
	tRT	Reset complete time	-	5 (note 1)		ms
			-	120(note 2)		ms

Note: (1) When reset applied during SLPIN mode;

(2) When reset applied during SLPOUT mode.

4.2 DSI Timing Characteristics
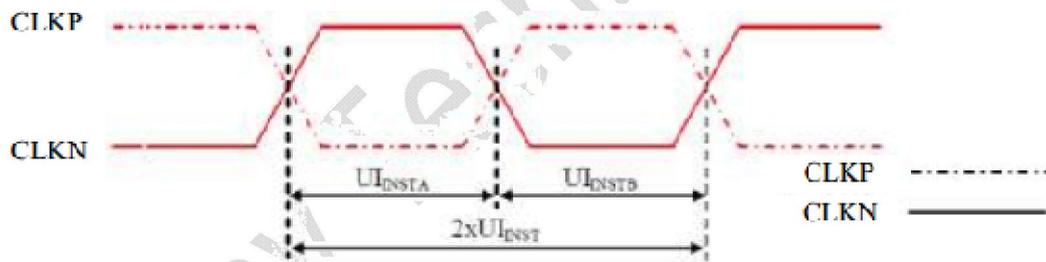
4.2.1 High Speed Mode － Clock Channel Timing

Figure 116: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2\times UI_{INST}$	Double UI instantaneous	Note 2	25	ns
CLKP/N	UI_{INSTA}, UI_{INSTB} (Note 1)	UI instantaneous Half	Note 2	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

2. Define the minimum value, see Table

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	466 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	525 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps

Limited Clock Channel Speed
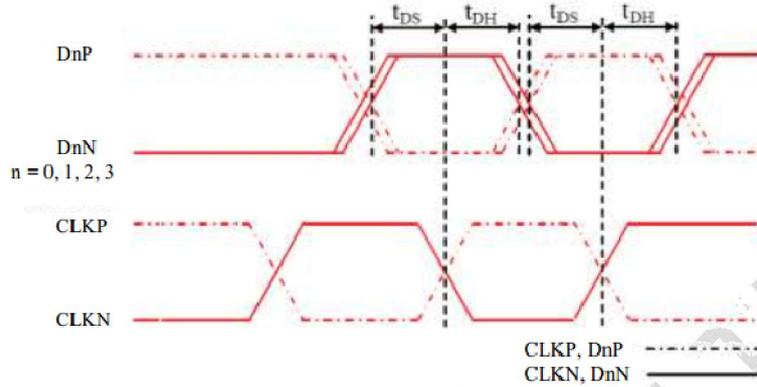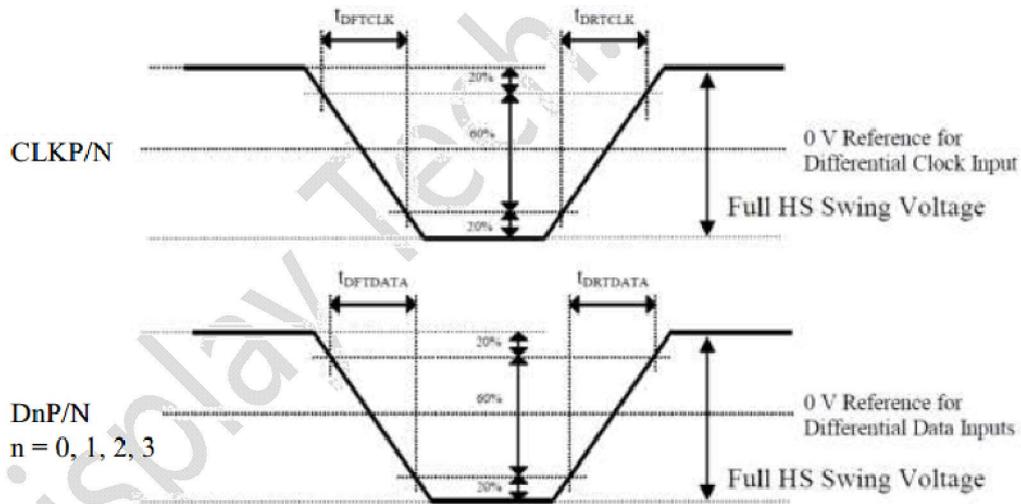
4.2.2   High Speed Mode － Data Clock Channel Timing

Figure 117: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

## 4.2.3   High Speed Mode － Rising and Falling Timings

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.

4.2.4   Low Speed Mode － Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C-0D) are illustrated for reference purposes below.
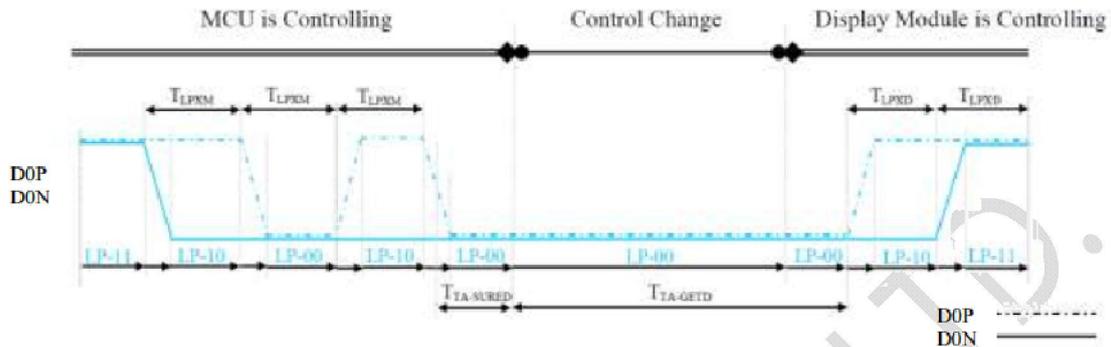
BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C-0D) to the MCU are illustrated for reference purposes below.
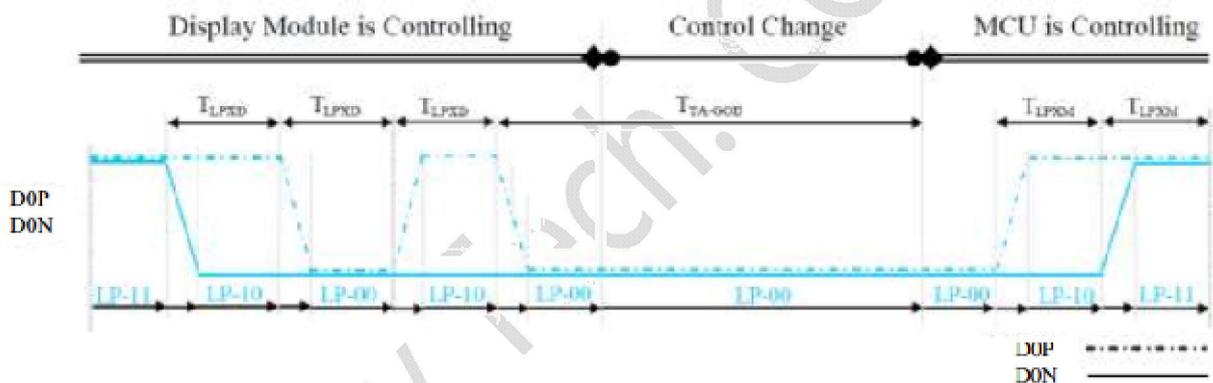

BTA from the Display Module to the MCU

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU ➜ Display Module (ILI9881C-0D)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C-0D) ➜ MCU	50	75	ns
D0P/N	$T_{TA\text{-}SURED}$	Time-out before the Display Module (ILI9881C-0D) starts driving	T_{LPXD}	$2 \times T_{LPXD}$	ns

Low Power State Period Timings – A

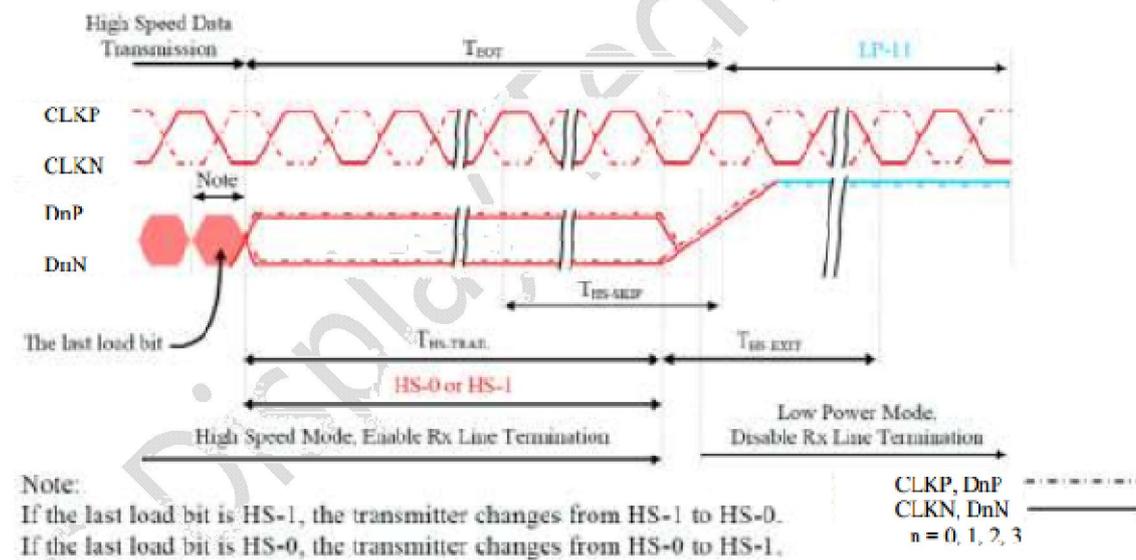| Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA\text{-}GETD}$	Time to drive LP-00 by Display Module (ILI9881C-0D)	$5 \times T_{LPXD}$	ns
D0P/N	$T_{TA\text{-}GOD}$	Time to drive LP-00 after turnaround request - MCU	$4 \times T_{LPXD}$	ns

Low Power State Period Timings – B

## 4.2.5   Data Lanes from Low Power Mode to High Speed Mode
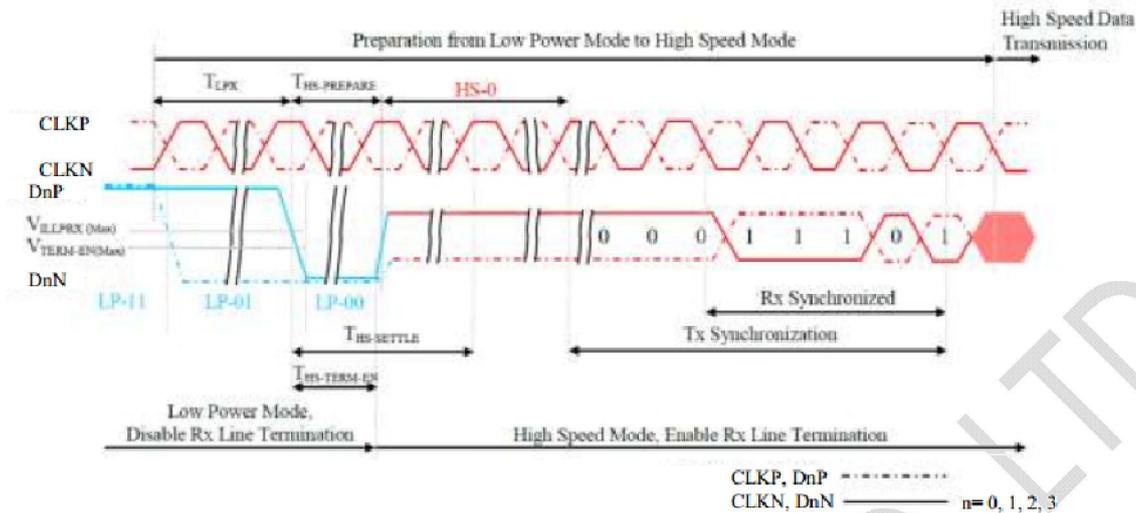
Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

4.2.6   Data Lanes from High Speed Mode to Low Power Mode

Note:
If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.
If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

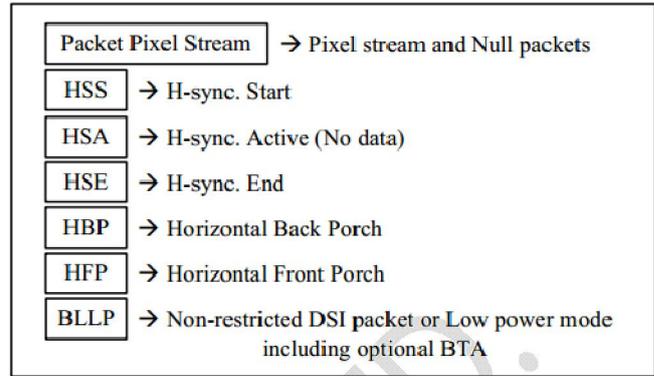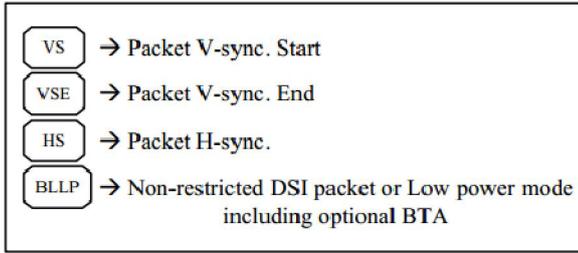| Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C-0D) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

4.2.7 DSI Clock Burst – High Speed Mode to/from Low Power Mode
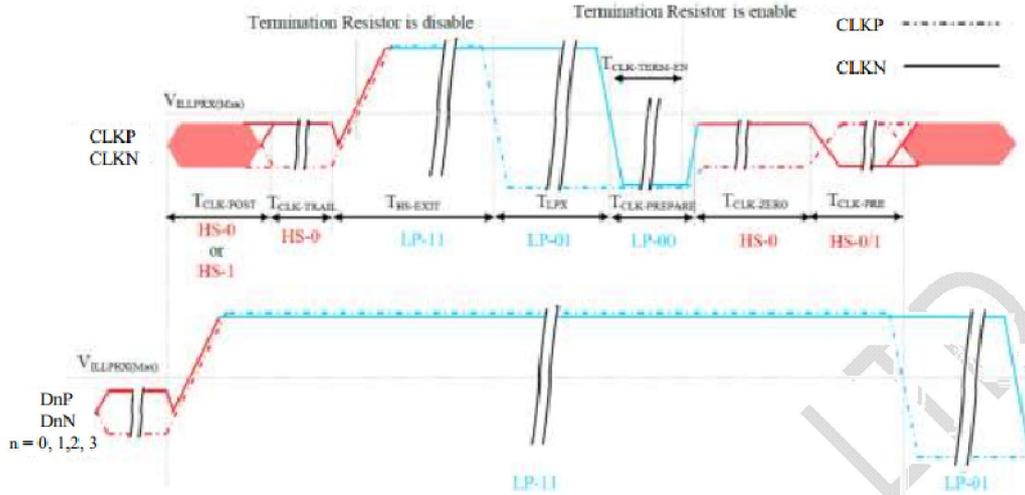
Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE}$ $+ T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

4.3 Timing for DSI video mode

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	→ Packet V-sync. Start
VS	→ Packet V-sync. Start
VSE	→ Packet V-sync. End
HS	→ Packet H-sync.
BLLP	→ Non-restricted DSI packet or Low power mode including optional BTA

Packet Pixel Stream	→ Pixel stream and Null packets
HSS	→ H-sync. Start
HSA	→ H-sync. Active (No data)
HSE	→ H-sync. End
HBP	→ Horizontal Back Porch
HFP	→ Horizontal Front Porch
BLLP	→ Non-restricted DSI packet or Low power mode including optional BTA

Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	2 (Note 6)	-	-	Line
Vertical Back Porch	VBP	14 (Note 6)	-	-	Line
Vertical Front Porch	VFP	8 (Note 6)	-	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	2	-	-	Pixel
Horizontal Porch period	HSA + HBP + HFP	1.6	-	-	us
Active pixels per line	HACT	-	720	-	Pixel
Bit rate	BR_{bps}	385		Note 5	Mbps/lane

1 UI=1/Bit rate

HSA(pixel)= (tHSA*lane number) / (UI* pixel format)

HBP(pixel)= (tHBP*lane number) / (UI* pixel format)

HFP(pixel)= (tHFP*lane number) / (UI* pixel format)

$$Frame\ Rate = \frac{BR_{bps}\ x\ Lane_{num}}{(VACT+VSA+VBP+VFP)\ x\ (HACT+HSA+HBP+HFP)\ x\ Pixel\ Format}$$

Example：BR$_{bps}$ = 457Mbps/lane, 1UI=2.1883ns, Frame rate=60Hz, VACT=1280, VSA=2, VBP=30, VFP=20, HACT=720, HSA=33, HBP=100, HFP=100, Lane$_{num}$=4(lane), Pixel Format=24(bit)

Note:

1. Lane$_{num}$: Date lane of MIPI-DSI.

2. Pixel Format: Please reference to "4.1DSI System Interface".

3. The formula exists slightly error because of the host-transmission way.

4. The best frame rate setting： 2 data lanes：50~60 Hz / 3 data lanes：50~70 Hz / 4 data lanes：50~70 Hz.

5. Please reference to "Table 39: Limited Clock Channel Speed".

6. The minimum values of this table mean the limitation of IC without considering the panel GIP. The actual values of VSA, VBP and VFP will be changed by different panel GIP setting

5   Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage (Analog)	VCC~GND	-0.3	7.0	V
Logic signal voltage(I/O)	IOVCC~GND	-0.3	3.8	V
Supply Voltage	VSP ~ GND	-0.3	7.0	V
Supply Voltage	VSN ~ GND	0.3	-7.0	V
Operating Temperature	TOP	-20	70	℃
Storage Temperature	TST	-30	80	℃
Humidity	RH	-	90%(Max 60°C)	RH

6   Electrical   Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Analog operating voltage	VCC	2.5	2.8	3.3	V
Logic operating voltage	IOVCC	1.65	1.8	3.3	V
Analog operating voltage	VSP	4.5	5.0	6.6	V
Analog operating voltage	VSN	-6.6	-5.0	-4.5	V
Input Current	IDD	-	TBD	-	mA
Input Voltage ' H ' level	VIH	0.7IOVCC	-	IOVCC	V
Input Voltage ' L ' level	VIL	GND	-	0.3IOVCC	
Output Voltage ' H ' level	VOH	0.8IOVCC	-	IOVCC	
Output Voltage ' L ' level	VOL	GND	-	0.2IOVCC	

7   Backlight   Characteristics

| ITEM	SYMBOL	MIN	TYP	MAX	UNIT
Voltage for LED backlight	V_f	-	18	18.6	V
Current for LED backlight	I_f	-	30	40	mA
Power consumption	Wbl	-	540	744	mW
Uniformity	Avg	80	-	-	%
LED Life Time	-	30000	40000	-	Hrs

Note:

1.The LED life time is defined as the module brightness decrease to 50% original brightness at Ta=25°C, 60%RH ±5 %.

2. The life time of LED will be reduced if LED is driven by high current, high ambient temperature and humidity conditions.

3. Typical operating life time is an estimated data.

4. Permanent damage to the device may occur if maximum values are exceeded or reverse voltage is loaded .Functional operation should be restricted to the conditions described under normal operating conditions.

8 LCD   Optical   specifications

| Item	Symbol	Condition	Specification			Unit	Remark
			Min	Typ	Max		
Response time (By Quick)	Tr+Tf	θ = 0°	-	30	35	ms	Note 1,3
Contrast ratio	CR	θ = 0°	640	800	-		Note 1,2
Viewing angle	Top	CR≧10	-	80	-	Deg.	Note 1,4
	Bottom	CR≧10	-	80	-		
	Left	CR≧10	-	80	-		
	Right	CR≧10	-	80	-		
Color chromaticity (CF only with ITO, light source is C light, CIE 1931)	Wx	θ = 0°	0.283	0.303	0.323		Note 1,4
	Wy		0.303	0.323	0.343		
	Rx		0.634	0.654	0.674		
	Ry		0.299	0.319	0.339		
	Gx		0.239	0.259	0.279		
	Gy		0.554	0.574	0.594		
	Bx		0.12	0.14	0.16		
	By		0.064	0.084	0.104		
Optima View Direction		free					Note 5

Note (1): Definition of viewing angle
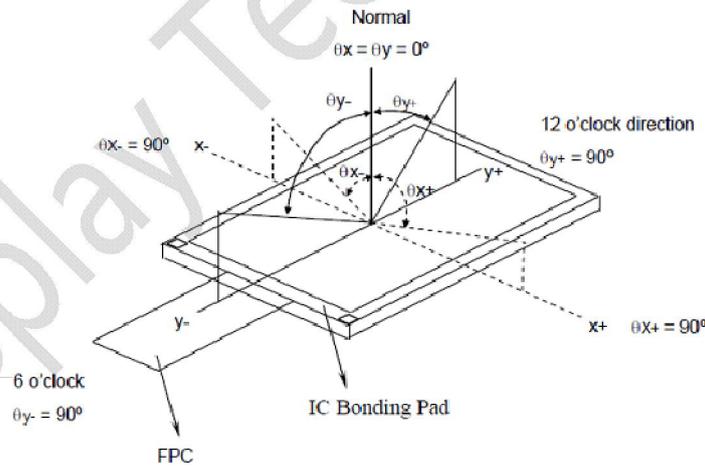
Note (2) Definition of Contrast Ratio (CR) :
measured at the center point of panel

$$CR = \frac{Luminance\ with\ all\ pixels\ white}{Luminance\ with\ all\ pixels\ black}$$
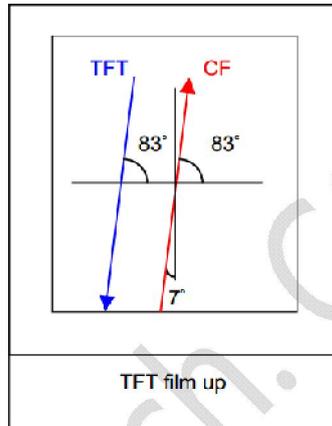
Note (3) Definition of Response Time: Sum of TR and TF
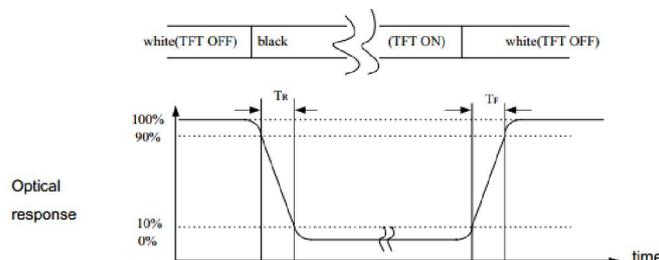
Note (4) Definition of optical measurement setup
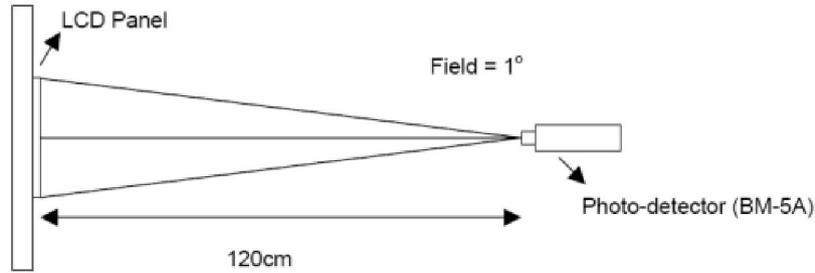
Note (5) Rubbing Direction (The different Rubbing Direction will cause the different optima view direction.)
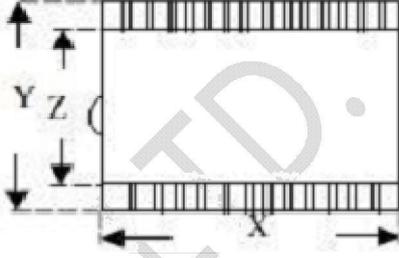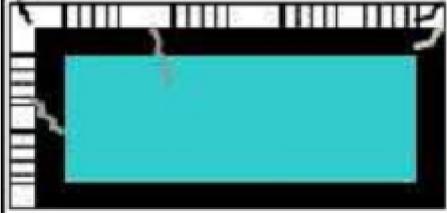

9 RELIABILITY TEST

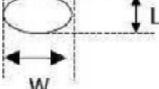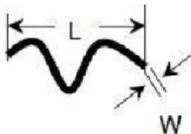| NO.	TEST ITEM	TEST CONDITION	INSPECTION AFTER TEST
1	High Temperature Storage	80±2°C/96 hours	Inspection after 2~4 hours storage at room temperature and humidity. The condensation is not accepted. The sample shall be free from defects: 1. Air bubble in the LCD 2. Seal leak 3. Non-display 4. Missing segments 5. Glass crack
2	Low Temperature Storage	-30±2°C/96 hours	
3	High Temperature Operating	70±2°C/96 hours	
4	Low Temperature Operating	-20±2°C/96 hours	
5	Temperature Cycle	-30±2°C ~ 25~ 80± 2°C × 10 cycles (30 min.) (5min.) (30min.)	
6	Damp Proof Test	60°C ±5°C × 90%RH/96 hours	
7	Vibration Test	Frequency 10Hz~55Hz Stroke: 1.5mm Sweep: 10Hz~150 Hz~10Hz 2 hours For each direction of X, Y, Z	
8	Shock Test	Half-sine, wave, 300m/s	
9	Packing Drop Test	Height: 80 cm 1 corner, concrete floor	
10	Electrostatic Discharge Test	C=150pF, R=330 Ω Air: ±8KV 150pF/330Ω 30 times Contact: ±4KV,20 times	

10 Inspection standards

10.1 Visual inspection criterion in cosmetic

10.1.1 Glass defect

NO.	Defect	Criteria	Remark
1	Dimension(Minor)	By engineering diagram	
2	Cracks(Major)	Extensive crack [Reject]	

10.1.2 LCM appearance defect

NO.	Defect	Criteria		Remark
		Spec	Permissible Qty	
1	Round type(Minor)	$\phi \leqslant 0.1mm$	Disregard	1. $\phi =(W+L)/2$, L:Length,W=Width 2.Disregard if out of A.A
		$0.1mm < \phi \leqslant 0.2mm$	2	
		$\phi > 0.2mm$	0	
2	Line type(Minor)	W $\leqslant 0.03mm$	Disregard	1. L:Length,W=Width 2.Disregard if out of A.A
		L$\leqslant$ 3.0mm and 0.03mm<W$\leqslant$0.05mm	2	
		L$\leqslant$ 3.0mm and 0.05mm<W$\leqslant$0.1mm	1	
		W>0.10mm or L>3.0mm	0	
3	Polarizer dent(Minor)	$\phi \leqslant 0.2mm$	Disregard	1. $\phi =(W+L)/2$, L:Length,W=Width 2.Disregard if out of A.A
		$0.2mm < \phi \leqslant 0.3mm$	2	
		$0.3mm < \phi \leqslant 0.5mm$	1	
		$\phi > 0.5mm$	0	

10.1.3 FPC

NO.	Defect	Criteria	Remark

| 1 | Copper peeling(Minor) | Copper peeling [Reject] | |
| 2 | Damaged | Damaged[Reject] | |

10.1.4 Black tape

NO.	Defect	Criteria	Remark
1	Shift(Minor)	IC exposed [Reject]	
2	No black tape(Minor)	No black tape [Reject]	

10.1.5 Silicon

NO.	Defect	Criteria	Remark
1	Amount of silicon (Minor)	ITO exposed [Reject]	

10.2 Visual inspection criterion in electrical display

NO.	Defect	Criteria		Remark
		Spec.	Permissible Qty	
1	No display (Major)	Not allowed		
2	Missing line (Major)	Not allowed		
3	Darker or lighter Line (Major)	Not allowed		
4	Weak line(Major)	By limited sample		
5	Bright / Dark point (Minor)	Bright point	1	1:1sub-pixel: 1R or 1G or 1B
		Dark point	2	2:Point defect area 1/2 sub pixel.
6	Round type (Minor)	$\phi \leq 0.1mm$	Disregard	1. $\phi =(W+L)/2$, L:Length,W=Width
		$0.1< \phi \leq 0.2$	3	2.Disregard if out of A.A
		$\phi >0.2mm$	0	
	Line type (Minor)	W $\leq 0.03mm$	Disregard	1. L:Length,W=Width
		L$\leq$ 3.0mm and 0.03mm<W$\leq$0.05mm	2	2.Disregard if out of A.A
		L$\leq$ 3.0mm and 0.05mm<W$\leq$0.1mm	1	
		W>0.10mm or L>3.0mm	0	
	Mura (Minor)	By 5% ND filter invisible		

10.3 Others

1. Issues that are not defined in this document shall be discussed and agreed with both parties. (Customer and supplier)

2. Unless otherwise agreed upon in writing, the criteria shall be applied to both parties. (Customer and supplier)

website: www.tslcd.com   www.lcdlcm.com   Email: tslcd@tslcd.com

11 Suggestions for using LCD modules

11.1 Handling of LCM

1. The LCD screen is made of glass. Don't give excessive external shock, or drop from a high place.

2. If the LCD screen is damaged and the liquid crystal leaks out, do not lick and swallow. When the liquid is attach to your hand, skin, cloth etc, wash it off by using soap and water thoroughly and immediately.

3. Don't apply excessive force on the surface of the LCM.

4. If the surface is contaminated, clean it with soft cloth. If the LCM is severely contaminated, use Isopropyl alcohol/Ethyl alcohol to clean. Other solvents may damage the polarizer. The   following solvents is especially prohibited: water , ketone Aromatic solvents etc.

5. Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets, moisture condensation or a current flow in a high-humidity environment.

6. Install the LCD Module by using the mounting holes. When mounting the LCD module make sure it is free of twisting, warping   and   distortion. In particular, do not forcibly pull or bend the I/O cable or the backlight cable.

7. Don't disassemble the LCM.

8. To prevent destruction of the elements by static electricity, be careful   to maintain an optimum work environment.

-   Be sure to ground the body when handling the LCD modules.

-   Tools required for assembling, such as soldering irons, must be properly grounded.

-   To   reduce   the amount of static electricity generated, do not conduct assembling and other work under dry conditions.

-   The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

9. Do not alter, modify or change the the shape of the tab on the metal frame.

10. Do not make extra holes on the printed circuit board, modify its   shape   or   change the positions   of components to be attached.

11. Do not damage or modify the pattern writing on the printed circuit board.

12. Absolutely do not modify the zebra rubber strip (conductive rubber) or heat seal connector

13. Except for soldering the interface, do not make any alterations or modifications with a soldering iron.

14. Do not drop, bend or twist LCM.

11.2 Storage

1. Store in an ambient temperature of 5 to 45   C, and in a relative humidity of 40% to 60%. Don't expose to sunlight or fluorescent light.

2. Storage in a clean environment, free from dust, active gas, and solvent.

3. Store in antistatic container.